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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,279	04/02/2004	Patrick J. Meaney	POU920030010US1	2306

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EXAMINER	
VIK, PHALLAKA	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,279	MEANEY ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to Applicant's amendment and drawings filed on 10/6/2006. Claims 1-10 are pending, wherein claims 1-7,9-10 have been amended.

Drawings

2. The drawings were received on 10/6/2006. These drawings are approved by the Examiner.

Claim Objections

3. **Claims 1-10** are objected to because of the following informalities:

As per **claim 1**, --logical-- should be inserted after "determining" (line 5) for proper antecedent basis for "the logical" (line 6); "the area" (line 9) should be --given an area-- for proper antecedent basis and for greater clarification.

As per **claim 2**, "the inputs" (line 7) should be --inputs-- for proper antecedent basis.

As per **claim 3**, "a static" (line 3) should be --static-- for proper grammar since "circuits" is plural.

As per **claim 2-5**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

As per **claim 6**, "for" (line 8) should be --of-- for proper grammar and to clearly define what is being claimed; "performing the total" (line 13) should be --by performing a total-- for proper antecedent basis and for greater clarification.

As per **claim 7**, --which-- should be inserted before "are" (line 4) for proper grammar.

As per **claim 8**, "the results" (line 3) should be --results-- for proper antecedent basis.

As per **claims 7-10**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. **Claims 2,4-5** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not understood what "establishing/determining an optimal mix of hierarchical level" means since Applicant's specification does not recite such terms. The closest description seems to be in paragraph [0018]; however, Applicant's claims do not these features so as to enable one skilled in the art to which it pertains to make and/or use the invention.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 2,4-5** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural/functional cooperative relationships of elements, such omission amounting to a gap between the necessary structural/functional connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: it is not understood what "optimal mix of hierarchical level" is since Applicant's specification does not use this term (see non-enablement rejection above) and there is no structural/functional relationship between the establishing step and the determining of the inputs step.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 1,3,6-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Watai et al.** (US Patent No. 5,745,373) in view of **Meaney et al.** (US Patent No. 5,996,040).

As per **claim 1**, **Watai et al.** discloses a method for providing an area optimized circuit system (col. 2, line 42-52) comprising the steps of:

determining the gate count for an implementation of a circuit system (col. 1, line 26-33; Figs. 3-4; col. 1, line 62 to col. 2, line 13; col. 2, line

19-30; col. 4, line 34-37),

and

minimizing the gate count and area needed to implement a circuit system given a library of logical gates to implement the circuit and the area for each gate in the library (Abstract; col. 1, line 26-33; col. 1, line 35-42; col. 3, line 4-10; Fig. 1, #106; col. 3, line 38-45; col. 3, line 51-59; Fig. 2; col. 4, line 18-37; col. 4, line 46 to col. 5, line 4; Figs. 3-4).

However, **Watai et al.** failed to specifically teach that the circuit system is a binary orthogonality checker for a scalable selector system for controlling data transfers and routing in a data processing system, as claimed. **Meaney et al.** disclose the method/circuit for implementing the binary orthogonal checker for a scalable selector system for controlling data transfers and routing in a data processing system (see col. 1, lines 15-21, 35-65). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further apply the circuit design process of **Watai et al.** to the particular binary orthogonal checker as taught by **Meaney et al.** so as to arrive at an integrated circuit implementing the binary orthogonal checker because such implementation would be at least optimized for area which in turn reduces manufacturing cost while still providing the desired binary othorgonal checker functionality.

As per **claim 3**, **Watai et al.** in view of **Meaney et al.** disclose all of the elements of claim 1, from which the claim depends, wherein **Watai et al.** further teaches the circuit being implemented in static CMOS circuits (see abstract; col. 1, line 26-33; col. 1, line

35-42; col. 3, line 4-10; Fig. 1, #106; col. 3, line 38-45; col. 3, line 51-59; Fig. 2; col. 4, line 18-37; col. 4, line 46 to col. 5, line 4.

Remarks

10. The objections of claims 1-4,6-10 due to the noted informalities are withdrawn in light of Applicant's amendment filed on 10/6/2006. However, as given above, claims 1-10 still contain informalities errors which were not completely corrected, newly introduced by Applicant's amendment and/or had not been raised by the previous Examiner.

11. The rejections of claims 6,7-10 under 35 U.S.C. 112, second paragraph, are withdrawn in light of Applicant's amendment filed on 10/6/2006 which corrected the errors. However, as per **claims 3,4-5**, the claims are still indefinite since it is not understood what "optimal mix of hierarchical level" is since Applicant's specification does not use this term (see paragraph [0018]) and there is no structural/functional relationship between the establishing step and the determining of the inputs step. There seems to be a misunderstanding of what the previous Examiner meant when he stated that there is "no existence determining of the optimal mix of hierarchical level" Although, Applicant has changed "determining" to --establishing--, such changes only causes more confusion than resolving the "existence of the 'optimal mix of hierarchical level" being established--in fact, "determining" is a better term than "establishing". Applicant should define the claims in terms of the steps involved in the specification as described in paragraph [0018] which the Examiner find is the closest thing to this determination of "optimal mix of hierarchical level". To further clarify the Examiner's

position, a non-enablement rejection is also given above since nowhere in the specification does Applicant describe "determining of optimal mix of hierarchical level".

12. The rejections of claims 1 and 3 as being unpatentable under 35 U.S.C. 102(b) are withdrawn in light of Applicant's arguments filed on 10/6/2006, wherein as pointed out by Applicant, **Watai et al.** failed to specifically teach the design of the orthogonal checker as claimed. However, as given in the new rejection above, **Watai et al.** (US Patent No. 5,745,373) in view of **Meaney et al.** (US Patent No. 5,996,040), **Watai et al.** is still applicable to Applicant's claimed invention since it provides a general method/system for implementing a circuit (which could also apply to orthogonal checker circuit) as taught in **Meaney et al.**, using the determined logical gate count and minimizing the logical gate count using a library of logical gates including the area of each logical gate, to implement the minimized circuit as claimed, wherein it would have been obvious to one of ordinary skilled in the art at the time of the invention to apply such teachings of **Watai et al.** to implement the orthogonal checker of **Meaney et al.** because such implementation would be at least optimized for area which in turn reduces manufacturing cost while still providing the desired binary othorgonal checker functionality.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Friday, 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner for Patents

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Alexandria, VA 22313-1450

or faxed to:

571-273-8300

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Phallaka Kik
Primary Examiner
December 26, 2006